SYNCHRONIZATION DETECTING APPARATUS

Background of the Invention

Field of the Invention

The present invention relates to a synchronization detecting apparatus for a wireless signal transmission line, which is comprised by a CDMA system receiver.

Description of the Related Art

A CDMA system attempts to improve its reception quality by using RAKE reception, which is path diversity (plus space diversity reception (antenna diversity reception)). In a signal format of a W-CDMA system, a synchronization signal (Sync Word: hereinafter referred to simply as an SW) for detecting synchronization is multiplexed on a pilot signal, and the SW is demodulated by a receiver to detect synchronization. The RAKE receiver makes estimation (channel estimation) for the state of a propagation path by using a pilot signal included in a reception signal containing a lot of noise, makes synchronization detection, and synthesizes paths so as to demodulate data.

Fig. 1 shows the configuration of a conventional

receiver.

In this figure, a synchronization detection process is performed for an SW signal multiplexed on a pilot signal and a data signal.

A signal input from an antenna 10 is converted into baseband signals by a demodulating unit 11, and these signals are further converted into digital signals by A/D converters 12-1 and 12-2. The converted signals are input to a despreading unit 13. Here, a CDMA despreading process is performed, and the despread signals are input to a synchronization detecting circuit 14-1 for demodulating data and a synchronization detecting circuit 14-2 for demodulating an SW. In Fig. 15, there are two systems of the synchronization detecting circuits 14-1 and 14-2 and channel estimating circuits 15-1 and 15-2, and a plurality of fingers are shown as a CDMA RAKE receiver. After a maximum ratio synthesizing unit 16-1 synthesizes the outputs of the fingers, an error correcting unit 17 performs an error correction process for the synthesized output. The data is then output. Similarly, after a maximum ratio synthesizing unit 16-2 synthesizes the outputs of the synchronization detecting circuit 14-2 for demodulating an SW at a maximum ratio, a synchronization detecting unit 18 performs a synchronization detection process for the

synthesized output to determine synchronization.

Additionally, actual channel estimating circuit and synchronization detecting circuits are configured to handle a signal to be processed as a complex baseband signal.

Fig. 2 exemplifies the format of a CDMA system frame.

1 frame is composed of 15 slots, and an SW is multiplexed on a pilot signal that is used when a reception signal is demodulated. Synchronization is determined by using the SW.

In the meantime, with a channel estimation method, channel estimation is made for example, by using pilot symbols in preceding and succeeding slots so as to improve the S/N ratio of a pilot signal, as shown in the configuration of a channel estimating circuit exemplified in Fig. 3. Within a slot, in-phase synthesis is made for a plurality of pilot signals from which a pilot pattern is removed. In-phase synthesis is also made for slots, and a channel estimation value for demodulation is generated by making synthesis with weight coefficients. The weight coefficients are varied depending on the state of a propagation path.

However, an SW itself is included in a channel estimation result when the SW is demodulated by using

a channel estimation result, which becomes a reference at the time of synchronization detection. Therefore, the correlation between a channel estimation result and an SW becomes strong depending on weight coefficients and the number of pilot symbols. As a result, an SW does not become erroneous (for example, the SW does not become erroneous by 99 percent) even if no signal is input. An SW is included in a pilot signal used for channel estimation. Therefore, if the number of bits of the SW included in the pilot signal becomes relatively large, channel estimation is made almost based on the SW. Consequently, the phase of a signal is rotated, etc. with reference to the SW. That is, the SW is handled as being correct. If a result of the channel estimation made by using a pilot signal indicates the degree of susceptibility to SW bits as described above, the correlation between a channel estimation result and an SW is referred to as being strong or weak.

Accordingly, if a portable terminal is powered down, a base station side determines that a communication is terminated based on the phenomenon that the portable terminal goes out of synchronization, and releases the channel allocated to the portable terminal. However, if an SW does not become erroneous even if the portable terminal is powered down, the base station

determines that the communication still continues although the portable terminal is actually powered down. Accordingly, a trigger for releasing the channel cannot be obtained despite a long wait, although the portable terminal must terminate the communication and the channel must be released.

Fig. 4 is a graph showing the error rate characteristic of a normal signal.

It is proved from this figure that if reception quality is deteriorated, an error rate and a non-error rate become equal, and the error rate results in 0.5. However, if weight coefficients shown in Fig. 3 are set to (1,1,1,1,1), the SW error rate results in a rate shown in Fig. 5 when an SW signal is demodulated. That is, the error rate results in 0.15 although reception quality is bad.

Furthermore, the error rate characteristic obtained when a signal is demodulated on the condition that the weight coefficients are set to 0,0,1,0,0 is shown in Fig 6. It is proved from this figure that the error rate is on the order of 0.05 although reception quality is bad.

As described above, the SW error rate is not deteriorated even if the reception quality is bad. If a process is performed in the belief of this phenomenon,

it is determined that an SW is correct and a misunderstanding such that a communication is being made arises, although radio waves are not transmitted from a portable terminal (the reception quality should be the worst because only noise is input), and only noise is input from an antenna.

Summary of the Invention

An object of the present invention is to provide a synchronization detecting apparatus that is not affected by a channel estimation result.

A synchronization detecting apparatus according to the present invention, which detects synchronization by using a pilot signal on which a synchronization signal is multiplexed, comprises a channel estimating unit making channel estimation by using the pilot signal from which at least the synchronization signal is removed; and a synchronization signal demodulating unit demodulating the synchronization signal by using a result of the channel estimation, wherein synchronization detection is made by using the demodulated synchronization signal.

According to the present invention, the correlation between a result of channel estimation using a pilot signal and a synchronization signal becomes weak,

thereby accurately detecting the presence/absence of a synchronization signal even when noise is mainly received in a non-communication state, etc.

Accordingly, a base station can always detect that a portable terminal terminates its communication. As a result, wastage such that an unnecessary channel is occupied does not occur.

Brief Description of the Drawings

Fig. 1 shows the configuration of a conventional receiver;

Fig. 2 exemplifies the format of a CDMA system frame;

Fig. 3 exemplifies the configuration of a channel estimating circuit;

Fig. 4 is a graph representing an error rate characteristic (No. 1);

Fig. 5 is a graph representing an error rate characteristic (NO. 2);

Fig. 6 is a graph representing an error rate characteristic (No. 3);

Fig. 7 shows a first preferred embodiment;

Fig. 8 shows a second preferred embodiment;

Fig. 9 shows a third preferred embodiment;

Fig. 10 shows a fourth preferred embodiment;

Fig. 11 shows the configuration of a receiver according to a preferred embodiment of the present invention;

Fig. 12 exemplifies the circuit configuration of a channel estimating unit;

Fig. 13 exemplifies the circuit configuration of a synchronization detecting unit;

Fig. 14 explains a fifth preferred embodiment according to the present invention;

Fig. 15 shows a CDMA receiver comprising a fading frequency estimating circuit, according to a sixth preferred embodiment of the present invention;

Fig. 16 exemplifies the configuration of a receiver according to a seventh preferred embodiment of the present invention (No. 1);

Fig. 17 exemplifies the configuration of the receiver according to the seventh preferred embodiment of the present invention (No. 2);

Fig. 18 exemplifies the configuration of the receiver according to the seventh preferred embodiment of the present invention (No. 3);

Fig. 19 shows the configuration of blocks of a weight coefficient selecting circuit; and

Fig. 20 exemplifies the configuration of the receiver according to the seventh preferred embodiment

of the present invention.

Description of the Preferred Embodiments

The following description omits the explanations of the same constituent elements as those of the receiver shown in Fig. 1.

In preferred embodiments according to the present invention, if the correlation between a channel estimation value and a SW bit is expected to be strong, the SW bit is removed from the channel estimation value to weaken the correlation with the SW bit to be demodulated. This is because an SW cannot be properly detected if the correlation between a channel estimation result and an SW bit to be demodulated is strong.

With the above described method, the correlation between a channel estimation value and an SW bit is removed, thereby properly detecting an SW.

Fig. 7 shows a first preferred embodiment according to the present invention.

This figure shows 1 slot of the channel estimating circuit exemplified in Fig. 3. If a symbol to be demodulated is a symbol P1 as shown in Fig.7, this symbol is demodulated with a channel estimation value using symbols P2 through P8 (1 slot is composed of 8 bits in this case) other than the symbol P1. Similarly, if a

symbol P2 is to be demodulated, this symbol is demodulated with a channel estimation value using the symbols other than the symbol P2. In this way, the correlation between the channel estimation value and the SW bit (the symbol P1 or P2 in the above provided example) is eliminated, whereby an error rate can be set to on the order of 0.5 in a state where no signal is input.

Fig. 8 shows a second preferred embodiment according to the present invention.

As shown in this figure, if 4 SW symbols are multiplexed on an actual pilot symbol, SW detection is enabled if the correlation between a channel estimation value and the 4 SW symbols is removed. However, this increases control complexity. Therefore, a channel estimation value is generated with pilot symbols other than the SW symbols, so that synchronization detection is made.

Namely, in the example shown in Fig. 8, symbols P1 to P4 are SW symbols, and a channel estimation value is calculated with symbols P5 to P8. That is, only the amplitude values of the symbols P5 to P8 are in-phase-synthesized by being assigned weights in accordance with the circuit configuration shown in Fig. 3.

Fig. 9 shows a third preferred embodiment according to the present invention.

As shown in this figure, a correlation is removed by not a pilot signal in a slot to be demodulated, but pilot symbols in preceding and succeeding slots. Namely, no process is performed for a slot 3 including an SW symbol to be demodulated, and the amplitude values of symbols in slots 1, 2, 4, and 5 are in-phase-synthesized by being assigned weights, so that a channel estimation signal is generated.

Fig. 10 shows a fourth preferred embodiment according to the present invention.

As shown in this figure, pilot symbols are divided into group each composed of 2 symbols, and a pilot signal including an SW symbol is not used for each group to make channel estimation, thereby removing the correlation between a channel estimation value and an SW.

Fig. 11 shows the configuration of a receiver according to a preferred embodiment of the present invention.

As shown in this figure, 2 conventional channel estimating circuits 20 for detecting synchronization and for demodulating data are put into one for common use, thereby reducing the circuit scale. As a result,

a signal received by an antenna 21 is converted into complex baseband signals I and Q, which are then converted into digital signals via A/D converters. The converted digital signals are despread by fingers, and channel-estimated by the channel estimating unit. Then, synchronization detection is made by using a channel estimation value, which is a result of the channel estimation, and a data signal and a synchronization signal are synthesized at a maximum ratio by maximum ratio synthesizing units 23-1 and 23-2. Thereafter, the data signal is error-corrected and results in a data output, whereas the synchronization signal is synchronization-detected and results in a synchronization output.

Fig. 12 exemplifies the circuit configuration of a channel estimating unit.

Pilot patterns are predetermined, and a different pattern is used depending on the number of symbols and a slot. In Fig. 12, $Dq \cdot \cos\theta$ and $Dq \cdot \sin\theta$ structure a complex baseband signal. Additionally, this figure shows that pilot symbols exist are assigned with 0 symbol. The complex baseband signal is multiplied by a predetermined pilot pattern by a pilot pattern canceling unit 30 to cancel the pilot pattern. As a result, the pilot pattern results in a state where "1" successively

exists if the amplitude does not change or the phase does not rotate. The pattern is input to a pilot averaging unit 31, which respectively adds 6 symbols of I and Q signals. The addition results are assigned weights and output by a pilot weight assigning unit 32. A maximum ratio synthesizing unit is arranged at a stage succeeding this circuit.

Here, according to the preferred embodiment of the present invention, a bit, a group, or a slot including an SW to be demodulated is subtracted at a stage preceding this circuit, and is not input to the channel estimating circuit shown in Fig. 12. This can be easily implemented by arranging a selector, a subtracter, etc. at the stage preceding the channel estimating circuit shown in Fig. 12, and by making the selector, the subtracter, etc. operate at the timing when a symbol, a group, or a slot including an SW to be demodulated is input.

Fig. 13 exemplifies the circuit configuration of a synchronization detecting unit.

A reception signal is input to a synchronization detecting unit as a complex baseband signal composed of I and Q signals after being demodulated. Here, a channel estimation value is complex-multiplied, and its result is output as a real axis component and an

imaginary axis component. The reason why multipliers and signals input thereto are complex in this figure is that a channel estimation value is complex-multiplied for a complex baseband signal. The complex multiplication is to reproduce the same arithmetic operation as complex number multiplication. The complex number multiplication is reproduced by assuming that the I and the Q signals are respectively the real and the imaginary components of an input signal, and also a channel estimation value is composed of real and imaginary components. Although its circuit becomes complex, the two orthogonal components of the signal itself can be handled as one complex signal, which facilitates the handling of this signal.

Additionally, the correlation between a channel estimation value and an SW symbol can be weakened by always setting to, for example, 1,1,1,1,1, the weight coefficients of a channel estimating circuit having a conventional configuration shown in Fig. 3 independently from the weight coefficients for demodulating data. If a comparison is made between the SW error rates shown in Figs. 5 and 6, deterioration of the SW error rate estimation is improved by setting the weight coefficients as described above.

Fig. 14 shows a fifth preferred embodiment

according to the present invention.

As shown in this figure, a receiver according to this preferred embodiment comprises a reception quality estimating circuit 40, and weakens the correlation between an SW bit and a channel estimation value by switching channel estimation weight coefficients for SW detection if signal quality is bad.

Furthermore, the process for weakening the correlation between a channel estimation value and an SW, which is referred to in the above described preferred embodiment, may be also performed only if a reception signal such as a packet transmission signal is proved to become a burst signal. By applying this method, the amount of the channel estimation process is expected to be reduced.

Fig. 15 shows a preferred embodiment of a CDMA receiver comprising a fading frequency estimating circuit, according to a sixth preferred embodiment of the present invention.

In this case, weight coefficients for channel estimation are controlled with a fading frequency. The reception characteristic can be improved by setting the weight coefficients to, for example, 0,0,1,0,0 if fading is high-speed, or by setting the weight coefficients to, for example, 1, 1, 1, 1, 1 if there is no fading.

However, with the weight coefficients in the case of high-speed fading, the correlation between a channel estimation value and an SW becomes significantly strong, which makes proper SW detection difficult. Therefore, the process for weakening the correlation between a channel estimation value and an SW according to the above described preferred embodiment is performed at the time of high-speed fading.

Figs. 16 through 18 exemplify the configuration of a receiver according to a seventh preferred embodiment of the present invention.

In this preferred embodiment, both a fading frequency estimating circuit and a reception quality estimating circuit are arranged, and weight coefficients settings are varied by using both a fading frequency and a reception quality as parameters.

That is, a plurality of weight coefficients are prepared, and switched and used with a change in the fading frequency in a similar manner as in the preferred embodiment shown in Fig. 15.

Additionally, as shown in Fig. 18, prepared weight coefficients are switched and used if reception quality is bad. As the reception quality becomes better, the weight coefficients are varied according to a fading frequency as shown in Fig. 17.

Furthermore, as shown in Fig. 16, channel estimation parameters vary according to the number of pilot symbols, fading speed, etc. It is effective that a plurality of parameters such as the number of error-tolerable SW bits for synchronization detection, the number of forward protection stages, the number of backward protection stages, etc. are prepared, and switched according to the channel estimation parameters.

Or, since the channel estimation parameters change according to the number of pilot symbols, fading speed, etc., it is also possible to manage by an upper layer the parameters such as the number of error-tolerable SW bits for synchronization detection, the number of forward protection stages, the number of backward protection stages, etc., and to vary the parameters depending on need.

In Fig. 16, the fading frequency estimating circuit and the reception quality estimating circuit are arranged. In addition, a synchronization detection controlling circuit determines the number of error-tolerable SW bits, the number of backward protection stages, the number of forward protection stages, etc. by using the channel estimation parameters as inputs, and inputs the determined parameters to a

synchronization detecting circuit, which detects synchronization according to the parameters.

Fig. 19 shows the configuration of blocks of a weight coefficient selecting circuit.

In the weight coefficient selecting circuit, weight coefficients 1 through n are prepared. Upon receipt of reception quality information, a selector selects a suitable weight coefficient, and outputs the selected coefficient to a channel estimating circuit of a channel estimating unit.

Fig. 20 exemplifies the configuration of the receiver according to the seventh preferred embodiment of the present invention.

If the correlation between a channel estimation value and an SW is strong, an SW does not become erroneous even if no reception signal exists. A diversity gain is further expected at the time of RAKE reception. As a result, an error rate becomes lower, and the state is apt to become a synchronization state only with noise but with no signal. Therefore, as shown in Fig. 20, a finger(?) reliability degree detecting circuit is arranged, the degree of reliability of an output from each finger is detected, outputs of fingers with high degrees of reliability are synthesized at a maximum ratio for SW signal demodulation, and SW detection is

made, so that a diversity gain is reduced in a state where there is no signal. Here, the degree of reliability of each finger is, for example, the strength of the correlation value output from each finger. It is determined that as the strength of the correlation value increases, so does the degree of reliability of reception. A finger with a high strength of the correlation value is selected, and the above described method is applied.

According to the present invention, the correlation between channel estimation and an SW is weakened, thereby properly detecting the SW.